REMARKS

This response to the Office Action mailed on November 10, 2003 cancels claims 1-26 and adds new claims 27-49. As a result, claims 27-49 now remain pending in the Application.

The Specification is amended as requested in the Office Action. Correction of this typographical error does not add any prohibited new matter.

Claims 1, 9, 17 and 25 were rejected under 35 USC § 102(e) as anticipated by Brown et al. (U.S. 6,046,817). Claims 3-5, 11-13 and 19-21 were rejected under 35 USC § 103(a) as unpatentable over Brown et al. Claims 2, 10, 18 and 26 were rejected under 35 USC § 103(a) as unpatentable over Brown et al. in view of Call et al. (U.S. 4,158,235). Claims 6-8, 14-16 and 22-24 were rejected under 35 USC § 103(a) as unpatentable over Teitenberg et al. (U.S. 6,421,769) in view of Brown et al

The Brown patent describes a buffer for a printer that can be accessed through an infra-red port, a parallel port, a serial port, or a network port (col. 5:4[1]). The buffer operates at relatively low input speeds of 2,400 bps to 4 Mbps (col. 8:59). The buffer memory holds entire print jobs (col. 6:1:4), which have highly variable sizes. Brown thus initially allocates only a small number and size of buffers, and then reconfigures them extensively later (col. 4:23-27). These conditions make it almost imperative that the buffers are implemented as a large undifferentiated pool of main RAM (col. 4:18-20).

The Call patent, filed in 1977, buffers from a higher-speed device, such as a hard disk, to a lower-speed device, such as a tape drive. (col. 1:19-27). Call's buffers are not assigned by circuitry or software to particular channels. Instead, each buffer is always connected to the in/out data busses for all ports (col. 2:23-25; Fig. 2:21A-21B[2]). The buffers are addressed associatively (col. 2:29-30) by association units (Fig. 2:13_1-13_N) according to names sent with the data; see Fig. 3:29 and col. 8:1-45. The complex system of commands for assigning incoming data would seem to preclude operation at modern high-speed communication rates;

[1] ---The colon notation refers to column and line numbers. For example, "col. 5:4" indicates col. 5 line 4 in the reference.
[2] ---The colon notion here refers to figure and reference numeral. Hence "Fig. 2:21A-21B" indicates Figure 2, blocks 21A and 21B.

see, e.g., the preceding passage, and col. 9:23-35. Note also that many signals in addition to the data signals congest the data busses; col. 6:29-35.

Teitenberg relates to network switches, and does not specifically concern buffer structures. Teitenberg mentions the NGIO protocol (col. 3:18), but appears to be otherwise irrelevant to the present invention.

Applicant's system is designed to buffer high-speed communications channels that have the same nominal input and output data rates. That is, the purpose of Applicant's buffers is to overcome bumps in the road---to overcome occasional caesuras and temporary ritardandos in an otherwise a-tempo transmission flow. The buffer structure is therefore desirably simple, with minimal pauses in the data flow for figuring out which data goes where. Applicant has conceived an uncomplicated set of buffers that each provide a predetermined adequate size for normal operation of one port. However, certain circumstances allow one port to borrow excess capacity from one or more other ports that are not currently in use. No reassignment commands interrupt data flow even briefly, and the only added path delay is a simple multiplexor.

New claim 27 reflects Applicant's concept in a way that differentiates it from the cited prior art. For example, multiple discrete buffer "units" include their own individual memories and separate dedicated port logics, whereas Brown's buffer has only a common pool of memory, and Call has common in/out data busses that feed all buffer units in parallel. Claim 27 also has a multiplexor having one input to a port logic and a second coupled to "the write block of another of the buffer units," for effectively coupling two buffer memories in series. Brown has no suggestion of such an arrangement. Call connects the buffer memories only in parallel, through data busses 21A-21B, and does not connect the output ("read block"; see Application Fig. 3) of one buffer memory to the input (write block, Fig. 3) of another buffer memory. Neither Brown nor Call teaches flow-control logic that can switch such a multiplexor between the recited input connections. Teitenberg, of course, does not remotely suggest any of these features.

New claims 28-36 depend from claim 27, and incorporate further features as well. For example, claim 29 recites a chain of at least three interconnected buffers, "another of the buffer units" of claim 27 being "the other buffer unit" of claim 28, which is in turn couplable through "another multiplexor" to the read block of a further of the buffer units.. Claim 29 contains a

formulation than generalizes to any number of chained buffer memories in a similar manner, but in differing terminology. The references do not suggest a chain of three or more buffers.

Claim 30 specifies more than two inputs in at least some of the multiplexors, allowing multiple orders of buffers in the chain, as described on page 13:1-3[3] of the Specification. Brown has no need of reordering, because he merely increases a unitary memory area to obtain more buffer space for a needy port. Call routes data from port busses directly to each buffer, and has no concept of operating the buffers serially, and therefore does not suggest different serializations thereof. Claim 31 speaks of discrete buffer memories (Specification, page 10:5); Brown teaches away from such units, many times expressing a preference for common pools of memory. Claims 32 and 33 include the "cross-bar switch" of Fig. 2 and page 6:7. Claims 34 and 35 recite the write logics of Fig. 2 and page 5:22-6:1. The references have no such logics "between [a] multiplexor and [a] memory" of individual buffer units, and do not use such logics to indicate "how much space remains" in a buffer.

Independent claim 37 is drawn to a system including the invention. Fig. 5 of the Drawing shows the host system, channels, and channel adapters, which are described on pages 15-17 of the Specification. The references do not show such systems. In addition, the recited buffer units distinguish the prior-art references for the same reasons as adduced in connection with claim 37. Claims 38-42 depend from claim 37 and incorporate all of its distinguishing features. Again the Teitenberg reference has no relevance to the "NGIO" recitation of claim 42, because that reference has no relevance to buffer structures.

Independent method claim 43 also embraces Applicant's concept of chainable serial buffer units. After data is disabled through the second-port buffer memory (see Specification, page 10:22-11:1), claim 43 switches data "from the output of the first buffer memory to an input of the second buffer memory." This serial rearrangement is not found in Call, whose buffers are always connected in parallel. Brown's system has no inkling of thus serializing different buffer areas, and his common-pool environment would not profit from such a concept.

Claims 44-49 depend from claim 49. Claim 44 specifies a serialization among at least three buffer memories, as described on page 11:10-16. Claim 45 particularizes the data flow

[3] --- This colon notation refers to page and line numbers. For example, "page13:1-3" indicates page 13, lines 1-3 in the Specification.

through at least two serialized buffer memories; again, Call's buffer units Fig. 2:15 always remain in parallel---as Applicant's do only before the switching operation---and Brown has neither parallel nor serial operation. Page 12:1-15 describes Applicant's concept of multiple ways of serializing the buffer memories so that "not all data follows the same path through the buffer memories"; claim 46. Neither Brown nor Call serialize at all. Page 5:22-6:1 describes how the flow-control logic receives information regarding available buffer space, as recited in claim 48.

Conclusion

For the above reasons, Applicant urges that the Application meets all statutory requirements, and respectfully requests reexamination and allowance. The Examiner is invited to telephone Applicant's attorney at (612) 373-6971 if desirable to facilitate prosecution of this Application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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